HEWLETT-PACKARD COMPANY
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12-27-04

PATENT APPLICATION

ATTORNEY DOCKET NO. 100048291-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Robert Bushey

Confirmation No.: 8285

Application No.: 09/896,793

Examiner: D. K. Singh

Filing Date: 06-28-2001

Group Art Unit: 2676

Title: SYSTEM AND METHOD FOR COMBINING GRAPHICS FORMATS IN A DIGITAL VIDEO PIPELINE

Mail Stop Appeal Brief-Patents
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Sir:

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on **10-28-2004**.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $500.00.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

( ) (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d) for the total number of months checked below:

( )	one month	$120.00
( )	two months	$450.00
( )	three months	$1020.00
( )	four months	$1590.00

( ) The extension fee has already been filled in this application.

(X) (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account **08-2025** the sum of **$500.00**. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

(X) I hereby certify that this correspondence is being deposited with the U.S. Postal Service as Express Mail, Airbill No. EV482745313US, in an envelope addressed to: MS Appeal Brief, Commissioner for Patents, P O Box 1450, Alexandria, VA 22313-1450.
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OR

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Number of pages:

Typed Name: Phyllis Ewing

Signature: _____

Respectfully submitted,

Robert Bushey

By _____

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Docket No.: 10004829-1
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Robert Bushey

Application No.: 09/896,793 Confirmation No.: 8285

Filed: June 28, 2001 Art Unit: 2676

For: SYSTEM AND METHOD FOR COMBINING GRAPHICS FORMATS IN A DIGITAL VIDEO PIPELINE Examiner: D. K. Singh

APPEAL BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This brief is in furtherance of the Notice of Appeal, filed in this case on October 28, 2004.

The fees required under § 1.17(f), and any required petition for extension of time for filing this brief and fees therefore, are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief contains items under the following headings as required by 37 C.F.R. § 41.37.

I. REAL PARTY IN INTEREST

The real party in interest for this appeal is:

Hewlett-Packard Development Company, L.P., a Texas Limited Partnership, having its principal place of business in Houston, Texas.

II. RELATED APPEALS, INTERFERENCES, AND JUDICIAL PROCEEDINGS

There are no other appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application

There are 25 claims pending in the application.

B. Current Status of Claims

1. Claims canceled: none
2. Claims withdrawn from consideration but not canceled: none
3. Claims pending: 1-25
4. Claims allowed: none
5. Claims rejected: 1-25

C. Claims On Appeal

The claims on appeal are claims 1-25.

IV. STATUS OF AMENDMENTS

Appellant filed a Response to Final Office Action on August 6, 2004, wherein no amendments were proposed. The Examiner responded to the Response to Final Office Action in an Advisory Action mailed September 28, 2004. In the Advisory Action, the Examiner indicated that the arguments presented therein did not place the application in condition for allowance. The claims are enclosed herein as Appendix A.

V. SUMMARY OF CLAIMED SUBJECT MATTER

A summary of the claimed subject matter is provided below with reference numerals and references to the specification and drawings. The summary is set forth in one exemplary embodiment as the language corresponding to claims 1, 10, 19, and 21. Discussions about recitations of these claims can be found at least at the cited locations in the specification and drawings.

According to claim 1, an image processor comprises a graphics pipeline (109 of the Figure, page 12, line 6 through page 13, line 21) including a first plurality of stages (111-115 of the Figure) configured to process a graphic object (110), a bit map image pipeline (100 of the Figure, page 10, line 10 through page 12, line 5) including a second plurality of stages (102-108 of the Figure) configured to process a bit-mapped image (101 of the Figure), and a selectively configurable interconnection matrix (140 of the Figure) defining an image path for providing selected outputs from one or more of said stages of one of said pipelines to selected inputs of one or more of said stages of the other of said pipelines (page 14, lines 8-24).

According to claim 10, a method of processing an image comprises the steps of selectively configuring a pipeline interconnection matrix (140 of the Figure) to establish an image path through one or more stages of a graphics pipeline and one or more stages of a bit map image pipeline (page 13, line 27 through page 14, line 7), and processing an image (101, 110 of the Figure) by transmission along said image path through at least one stage of each pipeline (page 14, line 18 through page 15, line 19).

According to claim 19, an image processor comprises a first pipeline (109 of the Figure) including a plurality of graphic image processors (111-115 of the Figure) for processing a graphic object (page 12, line 6 through page 13, line 21), a second pipeline (100

of the Figure, page 10, line 10 through page 12, line 5) including a plurality of bit map image processors (102-108 of the Figure) for processing a bit-mapped image, and a switch (140 of the Figure) for selectively connecting an output from any one of said processors to an input of any other one of said processors (page 14, lines 8-24).

According to claim 21, a processor comprises a first pipeline (109 of the Figure) including a first plurality of stages (111-115 of the Figure) configured to process a first object (page 12, line 6 through page 13, line 21), a second pipeline (100 of the Figure) including a second plurality of stages (102-108 of the Figure) configured to process a second object (page 10, line 10 through page 12, line 5), and a plurality of interconnects (140 of the Figure) that connects each stage of first plurality of stages with at least one other stage in the first pipeline and with a third plurality of stages in the second pipeline, and connects each stage of second plurality of stages with at least one other stage in the second pipeline and with a fourth plurality of stages in the first pipeline (page 14, lines 8-24).

VI. GROUNDS FOR REJECTION TO BE REVIEWED ON APPEAL

A. First Ground

Claims 1, 4-5, and 7-25 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over *Hong* (U.S. Patent No. 5,943,064) in view of *Nally* . (U.S. Patent No. 5,598,525).

B. Second Ground

Claims 2, 3, and 6 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over *Hong* in view of *Nally* and further in view of *Sturgess* (U.S. Patent No. 5,861,893).

VII. ARGUMENT

A. First Ground of Rejection

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success.

Finally, the prior art cited must teach or suggest all the claim limitations. See M.P.E.P. § 2143. Without conceding the other criteria, Appellant asserts that the Examiner's rejection of these claims does not satisfy the third criterion.

1. Claim 1

Claim 1 recites, in part, "an image processor comprising a selectively configurable interconnection matrix defining an image path for providing selected outputs from one or more of said stages of one of said pipelines to selected inputs of one or more of said stages of the other of said pipelines." The Examiner admits that *Hong* does not disclose at least these limitations. Office Action mailed June 8, 2004 at 3. The Examiner asserts that the attribute controller (233 of Figure 2) of *Nally* teaches these limitations. *Id.* *Nally* teaches that the cited attribute controller is a member of the pipeline (205 of Figure 2). *Nally* at Col. 9, lines 26-28. The attribute controller receives an input from the serializer (236 of Figure 2) and provides an output to both CLUT (234) and overlay control (230). *Id.* at lines 35-43. The attribute controller is not selectively configurable because its inputs and outputs are constant and fixed to the serializer, CLUT, and overlay control. In other words, the attribute controller always receives input from the serializer and always provides its output to the CLUT and overlay control. This is illustrated in Figure 2 by direct, unbroken lines and at Col. 9, lines 29-43. Accordingly, *Nally* does not teach a selectively configurable interconnection matrix, as recited by claim 1. Thus, the combination of *Hong* and *Nally* does not teach or suggest the above-recited feature of claim 1. Therefore, the Appellant respectfully asserts that for the above reasons claim 1 is patentable over the 35 U.S.C. § 103(a) rejection of record.

2. Claim 10

Claim 10 recites, in part, "selectively configuring a pipeline interconnection matrix to establish an image path through one or more stages of a graphics pipeline and one or more stages of a bit map image pipeline." The Office Action relies upon the rejection of claim 1 for the rationale in rejecting claim 10. Office Action mailed June 8, 2004 at 5. For the purpose of the present appeal, Appellant assumes that the Examiner is not relying on *Hong* to disclose the claimed pipeline interconnection matrix, and Appellant assumes that the attribute controller of *Nally* is being relied upon to teach this method element. *Nally* teaches that the cited attribute controller is a member of the pipeline (205 of Figure 2). *Nally* at Col. 9, lines

26-28. The attribute controller receives an input from the serializer (236 of Figure 2) and provides an output to both CLUT (234) and overlay control (230). *Id.* at lines 35-43. The attribute controller is not selectively configurable because its inputs and outputs are constant and fixed to the serializer, CLUT, and overlay control. In other words, the attribute controller always receives input from the serializer and always provides its output to the CLUT and overlay control. This is illustrated in Figure 2 by direct, unbroken lines and at Col. 9, lines 29-43. Accordingly, *Nally* does not teach selectively configuring a pipeline interconnection matrix, as recited by claim 10. Thus, the combination of *Hong* and *Nally* does not teach or suggest all of the claimed limitations. Therefore, the Appellant respectfully asserts that for the above reasons claim 10 is patentable over the 35 U.S.C. § 103(a) rejection of record.

3. Claim 19

Claim 19 recites, in part, "a switch for selectively connecting an output from any one of said processors to an input of any other one of said processors." The Office Action states that it relies upon the rejection of claim 4 for the rationale in rejecting claim 10; however, Appellant believes that the Examiner meant to rely on claim 1. For purposes of this appeal, Appellant assumes that the Examiner is not relying on *Hong* to disclose the claimed switch and that the attribute controller of *Nally* is being relied upon to teach this switch. *Nally* teaches that the cited attribute controller is a member of the pipeline (205 of Figure 2). *Nally* at Col. 9, lines 26-28. The attribute controller receives an input from the serializer (236 of Figure 2) and provides an output to both CLUT (234) and overlay control (230). *Id.* at lines 35-43. The attribute controller cannot switch the outputs or inputs, as its inputs and outputs are constant and fixed to the serializer, CLUT, and overlay control. In other words, the attribute controller always receives input from the serializer and always provides its output to the CLUT and overlay control. This is illustrated in Figure 2 by direct, unbroken lines and at Col. 9, lines 29-43. Thus, the combination of *Hong* and *Nally* does not teach or suggest "a switch for selectively connecting an output from any one of said processors to an input of any other one of said processors," as recited by claim 19. Therefore, the Appellant respectfully asserts that for the above reasons claim 19 is patentable over the 35 U.S.C. § 103(a) rejection of record.

4. Claim 21

Claim 21 recites, in part, "a plurality of interconnects that connects each stage of first plurality of stages with at least one other stage in the first pipeline and with a third plurality of stages in the second pipeline, and connects each stage of second plurality of stages with at least one other stage in the second pipeline and with a fourth plurality of stages in the first pipeline." The Office Action relies upon the rejection of claim 1 for the rationale in rejecting claim 21. Office Action mailed June 8, 2004 at 6. For the purpose of the present appeal, Appellant assumes that the Examiner is not relying on *Hong* to disclose the claimed plurality of interconnects, and Appellant assumes that the attribute controller of *Nally* is being relied upon to teach the above-recited feature. *Nally* teaches that the cited attribute controller is a member of the pipeline (205 of Figure 2). *Nally* at Col. 9, lines 26-28. The attribute controller receives an input from the serializer (236 of Figure 2) and provides an output to both CLUT (234) and overlay control (230). *Id.* at lines 35-43. The attribute controller is not a plurality of interconnects because it is a single structure with constant and fixed inputs and outputs to the serializer, CLUT, and overlay control. This is illustrated in Figure 2 by direct, unbroken lines and at Col. 9, lines 29-43.

Further, claim 21 recites that the plurality of interconnects "connects each stage of first plurality of stages with at least one other stage in the first pipeline." Such function is not performed by the attribute controller of *Nally*. For instance, the attribute controller of *Nally* does not connect each of a plurality of the stages in the graphics backend pipeline (205, Figure 2) to at least one other stage in the graphics backend pipeline. The attribute controller sits between the serializer and CLUT in the graphics backend pipeline and does not act to connect a plurality of components in the graphics backend pipeline either at its input or its output. With regard to the video backend pipeline (204, Figure 2), the attribute controller connects to only one component of that pipeline (overlay control, 230 of Figure 2). Accordingly, *Nally* does not teach or suggest, "a plurality of interconnects that connects each stage of first plurality of stages with at least one other stage in the first pipeline and with a third plurality of stages in the second pipeline, and connects each stage of second plurality of stages with at least one other stage in the second pipeline and with a fourth plurality of stages in the first pipeline," as recited by claim 21. Thus, the combination of *Hong* and *Nally* does not teach or suggest all of the claimed limitations. Therefore, the Appellant respectfully

asserts that for the above reasons claim 21 is patentable over the 35 U.S.C. § 103(a) rejection of record.

5. Claims 4, 5, 7-9, 11-18, 20, and 22-25

Dependent claims 4, 5, 7-9, 11-18, 20, and 22-25 each depend either directly or indirectly from respective independent claims 1, 10, 19, and 21, and, thus, inherit all of the limitations of those respective independent claims. Thus, the cited combination of *Hong* and *Nally* does not teach or suggest all claim limitations of claims 4, 5, 7-9, 11-18, 20, and 22-25. It is respectfully submitted that dependent claims 4, 5, 7-9, 11-18, 20, and 22-25 are allowable at least because of their dependence from their respective base claims for the reasons discussed above.

B. Second Ground of Rejection

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art cited must teach or suggest all the claim limitations. See M.P.E.P. § 2143. Without conceding the other criteria, Appellant asserts that the Examiner's rejection of these claims does not satisfy the third criterion.

Dependent claims 2, 3, and 6 each depend either directly or indirectly from independent claim 1 and, thus, inherit all of the limitations of independent claim 1. Thus, the cited combination of *Hong* and *Nally* does not teach or suggest all claim limitations of claims 2, 3, and 6. It is respectfully submitted that dependent claims 2, 3, and 6 are allowable at least because of their dependence from claim 1 for the reasons discussed above.

VIII. CLAIMS INVOLVED IN THE APPEAL

A copy of the claims involved in the present appeal is attached hereto as Appendix A. As indicated above, the claims in Appendix A do include the amendments filed by Appellant on March 10, 2004.

IX. EVIDENCE

No evidence pursuant to 37 C.F.R. §§ 1.130, 1.131, or 1.132 or entered by or relied upon by the examiner is being submitted.

X. RELATED PROCEEDINGS

No related proceedings are referenced in II. above, or copies of decisions in related proceedings are not provided, hence no Appendix is included.

Appellant has enclosed all fees believed due with this response. However, if a fee is due, please charge our Deposit Account No. 08-2025, under Order No. 10004829-1 from which the undersigned is authorized to draw.

Dated: December 22, 2004

Respectfully submitted,

By: _____

Michael A. Papalas
Reg. No. 40,381
Attorney/Agent for Appellant

(214) 855-8186

I hereby certify that this correspondence is being deposited with the United States Postal Service as Express Mail, Airbill No. EV482745313US in an envelope addressed to: MS Appeal Brief - Patents, Commissioner for Patents, Alexandria, VA 22313-1450.

Date of Deposit: 12-22-2004

Typed Name: Phyllis Ewing

Signature: _____

APPENDIX A

Claims Involved in the Appeal of Application Serial No. 09/896,793

1. (Original) An image processor comprising:

a graphics pipeline including a first plurality of stages configured to process a graphic object,

a bit map image pipeline including a second plurality of stages configured to process a bit-mapped image, and

a selectively configurable interconnection matrix defining an image path for providing selected outputs from one or more of said stages of one of said pipelines to selected inputs of one or more of said stages of the other of said pipelines.

2. (Original) The image processor according to claim 1 wherein each of said first plurality of stages is different from the others and is selected from among the group of stages including scan conversion, clipping, windowing to viewport, projection, and sorting.

3. (Original) The image processor according to claim 1 wherein each of said second plurality of stages is different from the others and is selected from among the group of stages including demosaicing, color correction/white balancing, gamut mapping, tone correction, flare correction, color transformation, and scaling.

4. (Original) The image processor according to claim 1 further comprising an output stage connected to an output from each of said pipelines.

5. (Original) The image processor according to claim 1 wherein said interconnection comprises a switching matrix configurable to:

route outputs from one or more of said first plurality of stages to a next one of said first plurality of stages or to a selected one of said second plurality of stages; and

route outputs from one or more of said second plurality of stages to a next one of said second plurality of stages or to a selected one of said first plurality of stages.

6. (Original) The image processor according to claim 1 wherein said graphics pipeline is configured to receive graphics data including graphics identification and location data and said bit-mapped image pipeline is configured to receive a raster scanned image data representing pixel luminance information.

7. (Original) The image processor according to claim 1 further comprising a data format converter configured to convert between a graphics data format and a bit-mapped image data format.

8. (Original) The image processor according to claim 1 further comprising an image recognition stage configured to identify and encode graphic images within said bit-mapped image.

9. (Original) The image processor according to claim 1 further including a common instruction decoder operable to control said interconnection to route at least one of said graphic object and said bit-mapped image object between both said graphics and bit-mapped image pipelines.

10. (Original) A method of processing an image comprising the steps of:

selectively configuring a pipeline interconnection matrix to establish an image path through one or more stages of a graphics pipeline and one or more stages of a bit map image pipeline; and

processing an image by transmission along said image path through at least one stage of each pipeline.

11. (Original) The method according to claim 10 wherein processing performed by each of said stages of said graphics pipeline is different from processing performed by the others and is selected from among the group of processing including scan conversion, clipping, windowing to viewport, projection, and sorting.

12. (Original) The method according to claim 10 wherein processing performed by each of said stages of said bit map image pipeline is different from processing performed by the others and is selected from among the group of processing including demosaicing, color correction/white balancing, gamut mapping, tone correction, flare correction, color transformation, and scaling.

13. (Original) The method according to claim 10 further including a step of combining outputs from each of said pipelines into a merged output.

14. (Original) The method according to claim 10 wherein said step of selectively configuring said pipelines includes one of:

alternatively routing outputs from one or more stages of one of said pipelines to a next one of said stages or to a selected one of said stages of the other pipeline.

15. (Original) The method according to claim 10 wherein further including steps of passing graphics data including graphics identification and location data to said graphics pipeline and passing raster scanned image data representing pixel characteristic information to said bit map image pipeline.

16. (Original) The method according to claim 10 further comprising a step of converting between a graphics data format and a bit-mapped image data format.

17. (Original) The method according to claim 10 further comprising a step of image recognition including identification and encoding of said graphic images within said bit-mapped image.

18. (Original) The method according to claim 10 further including a step of controlling an interconnection to route at least one of said graphic object and said bit-mapped image object between both said graphics and bit map image pipelines.

19. (Original) An image processor comprising:

a first pipeline including a plurality of graphic image processors for processing a graphic object,

a second pipeline including a plurality of a bit map image processor for processing a bit-mapped image, and

a switch for selectively connecting an output from any one of said processors to an input of any other one of said processors.

20. (Original) The image processor according to claim 19 wherein:

a processing function performed by each of said graphic processors is different from a processing function performed by any other graphic processor and at least one of said processing functions is selected from among the group of processes including scan conversion, clipping, windowing to viewport, projection, and sorting; and

a processing function performed by each of said bit map image processor is different from a processing function performed by any other bit map processors, processing functions is selected from among the group of processes including demosaicing, color correction/white balancing, gamut mapping, tone correction, flare correction, color transformation, and scaling.

21. (Previously Presented) A processor comprising:

a first pipeline including a first plurality of stages configured to process a first object,

a second pipeline including a second plurality of stages configured to process a second object, and

a plurality of interconnects that connects each stage of first plurality of stages with at least one other stage in the first pipeline and with a third plurality of stages in the second pipeline, and connects each stage of second plurality of stages with at least one other stage in the second pipeline and with a fourth plurality of stages in the first pipeline.

22. (Previously Presented) The processor of claim 21 further comprising:

a converter configured to convert between a data format of the first object and a data format of the second object.

23. (Previously Presented) The processor of claim 21 further comprising:

a recognition stage configured to identify and encode the first object within the second object.

24. (Previously Presented) The processor of claim 21 further comprising:

an output stage connected to an output from each of the pipelines.

25. (Previously Presented) The processor of claim 24 further comprising:

a final stage of the first pipeline that is connected to each stage of the second plurality of stages and the output stage; and

a final stage of the second pipeline that is connected to each stage of the first plurality of stages and the output stage.